-crystallizing the semiconductor film by heating,
-patterning the crystalline semiconductor film to an active layer including the selected portion,
-forming a gate insulating film over the active layer,
-forming a gate electrode over the gate insulating film, forming an insulating film over the gate insulating film, and
-forming a wiring over the insulating film, **wherein the wiring is connected to the selected portion**. (Emphasis added)

A review of the Oka reference, particularly the full English translation, and Figures 1(c), 1(d), 2(c), 2(d), 3(a), 3(b), 4, and 5, reveals that Oka does not teach, either implicitly or explicitly, each feature of the independent claims. Specifically, the Examiner states, at page 3 of the Office Action, that Oka discloses "forming an insulating film (FIG. 1(d), element 109) over the gate insulating film; and forming a wiring (FIG.1(d), element 111) over the insulating film, **wherein the wiring is connected to the selected portion...**" However, a detailed review of Oka reveals that the document does not teach this latter step, in that the "selected portion" of Oka referred to by the Examiner is the in fact the seed region (FIG. 1(c), element 104; FIG. 2(c), element 204; FIG 3(b), element 203; FIG. 3(c), element 204; FIG. 4, element 403; FIG. 5, element 503) which in every embodiment Oka does not form any part of the active device region at all.

That is, Oka teaches, in a first embodiment, forming the seed regions at the periphery of the intended device area (FIG 1(c), elements 104), and, after seed growth, patterning the crystallized semiconductor to remove the periphery of the intended device area (Translation, page 8, lines 10-11) to form the semiconductor islands (FIG. 1(d), element 105) which are to form the active device regions (FIG. 1(d), elements 107) that receive the wiring connections (FIG 1(d), elements 111). In an alternative embodiment, Oka teaches an initial patterning step (Translation, page 11, lines 13-17) to form the amorphous semiconductor material into the semiconductor islands (FIG. 2(c), element 205) and to form the seed regions (FIG. 2(c)-3(b), elements 203) connected at the periphery of the semiconductor islands (FIG. 3(b), element 205) via a

connecting bridge (FIG. 3(b), elements 206). Thereafter, after crystallization to form the crystallized semiconductor islands (FIGS. 4, 5; Translation page 11, line 23, to page 12, line 18), the active device regions (FIG. 2(d), elements 205) are formed by again patterning, by the same TFT method of the first embodiment (Translation, page 8, lines 10-11; page 12, lines 19-26, i.e., "The method of formation of TFT can be the same method as in the application example of Figure 1."), the previously patterned semiconductor island (FIG 2(c), element 205) to remove the periphery regions, which includes the seed regions, and form the active device regions (compare FIGS. 2(c), 2(d)) with the wiring connected to the active device regions and not to the seed regions, as presently claimed.

As can be appreciated by one of ordinary skill in the prior art, each process of forming TFT devices in Oka appreciates the patterning to remove the peripheral seed regions prior to forming the semiconductor islands which are to become the active device regions, and in each instance the wiring connections are made to the active portions of the remaining crystallized semiconductor island which does not include the seed region. For these reasons, the Oka patent document does not teach each feature of the invention set forth in the independent claims 85, 91, 97, 103, 109 and 115 and, therefore, anticipation cannot exist. Consequently, the rejection of claims 85-87, 90-93, 96-99, 102-105, 108-111, 114-117 and 120, under §102(b), over the teachings of Oka has been set forth in error and should be withdrawn.

Turning to the Kuznetsov article, a review of that article reveals that the author merely teaches specific concentrations for the crystallization promoting Ni formed in patterns on the a-Si substrate which, upon heating, promotes the lateral diffusion/crystallization of the silicon (stated by the Examiner to be inherent in Oka). Such a teaching does not in any manner cure the failure of Oka to teach forming the wiring connections to the seed (selected) portions of the active regions as presently claimed and certainly provides no motivation to one of ordinary skill in the prior art to

modify the teachings of Oka so as not to remove the peripheral seed regions of Oka and instead utilize the seed regions as part of the active device regions, i.e., source/drain regions, to which the wiring connections are to be formed. For these reasons, a *prima facie* case of obviousness has not been established with regard to the teachings of Oka and the Kuznetsov article, and, consequently, the rejection of claims 88, 89, 94, 95, 100, 101, 106, 107, 112, 113, 118 and 119, under §103(a), has also been set forth in error and must now be withdrawn.

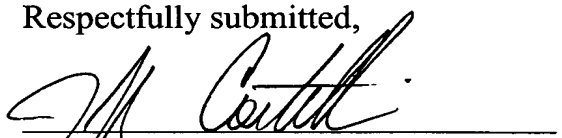
Finally, if the Examiner is to maintain, in the next office action, the position that Oka does in fact teach "forming an insulating film (FIG. 1(d), element 109) over the gate insulating film; and forming a wiring (FIG.1(d), element 111) over the insulating film, wherein the wiring is connected to the selected portion...," then the Applicants specifically request that the Examiner provide a reasoned technical explanation and supporting evidence (in Oka or other documentation) that Oka does in fact teach leaving the seed portions intact after crystallization and then teaches using the seed portion for the active regions of the semiconductor device, including forming wiring connections to the seed portions (i.e., the "selected portion" of the instant independent claims).

Thus, Applicants respectfully request consideration and allowance of the present application for the reasons provided above, i.e., it is submitted that claims 85-120 are now in condition for allowance. An early and favorable Notice of Allowance is respectfully solicited. In the event that the Examiner is of the opinion that a brief telephone or personal interview will facilitate allowance of one or more of the above claims, the Examiner is courteously requested to contact Applicants' undersigned representative.

Lastly, it is noted that a separate Extension of Time Petition (one month) accompanies this Response along with an authorization to charge the requisite extension of time fee to Deposit Account No. 19-2380 (740756-1641). However,

should that petition become separated from this Response, then this Response should be construed as containing such a petition. Likewise, any overage or shortage in the required payment should be applied to Deposit Account No. 19-2380 (740756-1641).

Respectfully submitted,



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